SEMICONDUCTOR MEMORY DEVICE

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Abstract of **JP63115369**

PURPOSE:To enable a high-speed operation by forming a double-layer film composed of a silicon oxide film and an insulating film having a dielectric constant higher than the silicon oxide film in part of the Schottky barrier diode (SBD) of the memory cell section, and adding a MIS capacity CSIN due to the bouble-layer film in parallel with the SBD capacity, thereby enhancing the degree of integration and the reliability.

CONSTITUTION:A base region and a region becoming a resistance are formed, an oxide film 7 is formed, and thereafter a silicon nitride film is formed thereon. Then leaving a silicon nitride film 18 in part of a SBD 9a, the remainder is etched away, and thereafter the oxide film 7 is etched for opening the contact hole of the emitter, base, collector and SBD parts. And arsenic is implanted into the part becoming an emitter region, a heat treatment is performed to form a N<+> layer, and thereafter the formation is performed according to the prior art process. Since in a semiconductor memory device consisting of such construction, a MIS capacity CSIN due to a double-layer film comprised of the oxide silicon oxide film 7 and a silicon nitride film 18 of a high dielectric constant is placed in parallel with the SBD 9a of the memory cell, the total capacity C becomes large, so it becomes strongly resistant to the information reversal of the memory cell due to alpha-ray or the like. Also, since CSIN is not placed in the peripheral circuit part, the parasitic capacity does not increase, enabling a high-speed operation.